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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,985	04/12/2004	Masayuki Koyama	70456-028	2075

7590 05/03/2006

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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,985	KOYAMA, MASAYUKI	
	Examiner	Art Unit	
	Ernest Unelus	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/821,985 has a total of 8 claims pending in the application; there is 1 independent claim and 7 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on applications filed on December 1, 2003 (Japan 2003-401301).

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated April 12, 2004 is acknowledged by the examiner and the

cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-8**, are rejected under 35 U.S.C. 102(b) as being anticipated by Ganapathy et al. (US 2002/0038393).

7. As per **claim 1**, Ganapathy discloses a direct memory access controller **(see fig. 2)**, comprising: a plurality of direct memory access transfer portions **(core processors 202A-202N)** controlling direct memory access transfer in accordance with values set in a group of registers for current transfer **(paragraphs 0020 and 0029 discloses values, which is instruction, set in a group of registers for current transfer)**; and a control portion **(bus arbitrators 201A-201N)** permitting use of a bus by said plurality of direct memory access transfer portions in a prescribed order **(round-robin)** such that bus ownership is passed among channels **(connection between the bus master (203A-**

203N) and the system bus (200)) at every prescribed number of transfers **(paragraphs 0019 and 0029)**, in response to transfer requests from said plurality of direct memory access transfer portions **(paragraph 0020 discloses transfer requests from the said plurality of direct memory access transfer portions, 202A-200N)**, while the bus ownership is granted from a bus master **(bus master 203A-203N, see fig. 2 and paragraph 0019)**.

8. As per **claim 2**, Ganapathy discloses a direct memory access controller according to claim 1**(see claim I above)**, "further comprising a group of registers for next transfer **(DMA descriptor registers in the DMA controllers 203, which are inside the processor (202), one of the plurality of direct memory access transfer portions, see paragraph 0029)**; wherein said direct memory access transfer portions transfer values **(paragraphs 0020 and 0029 discloses values, which is instruction, set in a group of registers for current transfer)** set in said group of registers for next transfer to said group of registers for current transfer to control direct memory access transfer **(paragraph 0029 discloses, "the instructions for DMA transfer between a data memory 302 and the global buffer memory 210 include start, stop, continue, suspend, and resume. There are DMA descriptor registers in the DMA controllers 203. One or more of these instructions can be written into the DMA descriptor registers while the DMA is in progress and can cause the appropriate action to be performed")**.

9. As per **claim 3**, Ganapathy discloses wherein to said group of registers for next

transfer **(DMA descriptor registers in the DMA controllers 203, which are inside the processor (202), one of the plurality of direct memory access transfer portions, see paragraph 0029)**, direct memory access control information stored in an external memory is successively transferred and stored **(paragraphs 0023 and 0024 discloses an external host, which will serve as the external memory, to transmit and receive data)**.

10. As per **claim 4**, Ganapathy discloses wherein transfer of the direct memory access control information from said external memory to said group of registers for next transfer is performed after values stored in said group of registers for next transfer are transferred to any of said plurality of direct memory access transfer portions and before bus ownership is switched among said plurality of direct memory access transfer portions **(paragraph 0025 discloses "In any case, the data that needs processing is stored into the global buffer memory 210 first. The one or more core processors 202A-202N then retrieve the data for the given channel for processing")**.

11. As per **claim 5**, Ganapathy discloses wherein said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with round robin method **(paragraph 0019 discloses "A round-robin arbitration scheme on the system bus 200 assures that each of the distributed DMA master controllers 203A-203N, 207 and 215 have access every so often to the system bus 200 and can access the global memory 210 at that time")**.

12. As per **claim 6**, Ganapathy discloses wherein said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with past number of direct memory access transfers by each channel **(paragraph 0037 discloses "the data is time division multiplexed on the serial data stream into time slots for each communication channel. Because the distributed DMA of the present invention is particularly suited to support blocks of data for given channels, the serial port provides interleaving and deinterleaving of data from the serial data stream for each channel")**.

13. As per **claim 7**, Ganapathy discloses wherein in said control portion **(bus arbitrators 201A-201N)**, number of transfers made by each channel while one continuous bus ownership is being granted is set **(paragraph 0038)**, and said control portion permits use of the bus among said plurality of direct memory access transfer portions in accordance with said number of transfers **(paragraph 0038, this is done using the round-robin)**.

14. As per **claim 8**, Ganapathy discloses wherein in said control portion **(bus arbitrators 201A-201N)**, an order of bus **(round-robin)** use by channels is set when there are three or more channels **(Ganapathy discloses multiply channels, for example, connections between the bus master (203A-203N) to the system bus (200), see fig. 2)**, and bus **(200)** use is permitted among said plurality of direct memory access transfer portions **(core processors 202A-202N)** in accordance with the order **(round-robin)** of bus use **(paragraph 0019)**.

VI. RELEVANT ART CITED BY THE EXAMINER

15. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

16. The following reference teaches a direct memory access controller comprising a plurality of direct memory access transfer portions.

U.S. PATENT NUMBER

US 6,701,405

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

17. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

17. Per the instant office action, claims 1-8 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-

8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

19. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 24, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

Ernest Unelus
Examiner
Art Unit 2187